Remarks

Claims 1, 3-17, 19-22, and 24-33 are pending. Claims 1, 3-6, 10-17, 19-22, and 24-33 stand rejected. Claims 7-9 stand objected to. No claims are added or canceled by amendment. Accordingly, claims 1, 3-17, 19-22, and 24-33 are at issue. Further examination or reconsideration is requested.

Claims 17, 19-22, and 25 stand rejected under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement. Applicants respectfully traverse the rejection.

In contrast to the position taken on page two of the November 27, 2007 Office Action, the claimed feature that "input samples for the IFFT are not multiplied by rotator coefficients" is fully supported by the specification. The written description discloses at least two alternative ways to modify an IFFT to perform a circular shift without a discrete step of multiplying input data samples by rotator coefficients.

In conventional IFFT pipelines, the butterfly units output the result of the addition first, and output of the subtraction second. The present application discloses that changing the order of these operations, under certain circumstances, can cause a circular shift. This change is accomplished by appropriate change in the control circuitry and memory contents of the multiplier circuit with memory for the IFFT butterfly pipeline. For example, it is explained in paragraphs 0059-0065 that for certain cases, the circular shift may be obtained by modifying twiddle factor coefficients and the control for the rotator circuits. In another example, it is explained in paragraphs 0066-0072 that controls may be modified to change the order of the operations so that the output of the subtraction operation of the butterfly circuit is output first, and the output of the addition operation is output second. Either of these modifications, along with modifications to the controls for the rotator circuits, can implement a desired circular shift without a separate multiplication step added before the IFFT circuitry to modify input samples with rotator coefficients.

As the November 27, 2007 Office Action points out, in the alternative embodiment in Fig 13, when elements 202 and 206 (Fig. 12) are eliminated, there is still a multiplier 226. However, a conventional IFFT pipeline may also have multipliers. See, for example, Fig. 10 and Fig. 11. However, the multipliers in known IFFT pipelines are not know in prior art to be configured or controlled to cause a circular shift of the data samples. Additionally, twiddle factor multiplier 226 in Fig. for the IFFT pipeline is not the same as a rotator coefficient multiplier at the input of the IFFT

pipeline because no rotator coefficients are provided to the multiplier 226. For the above reasons, claims 17, 19-22, and 25 are believed supported by the written description.

Claims 1 and 21-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni et al., U.S. Pub. No. 2004/0151110, in view of admitted prior art. Applicants respectfully traverse the rejection.

The November 27, 2007 Office Action is mistaken when it states that Mazzoni discloses a fast Fourier transform circuit adapted "to circularly shift the input data by m samples." This is incorrect because in Mazzoni, the fast Fourier transform circuit itself is not configured to circularly shift anything. Instead, in Mazzoni, a separate multiplier (reference numeral 22) is provided to **multiply the input samples with rotator coefficients *before* the data samples are input to the fast Fourier transform circuit**. As discussed above with respect to the rejection based on 35 U.S.C. §112, in the present invention, the IFFT pipeline is modified in such a way to provide a new IFFT pipeline that achieves a circular shift by altering the memory contents and controls for the various structures inside the IFFT pipeline so that a circular shift can be achieved without an external rotator coefficient multiplier.

Claim 1, as presently amended, recites that the Inverse Fast Fourier Transform circuit itself is adapted to circularly shift the input data by m samples. Because Mazzoni and the prior art described in the present application fail to disclose all of the elements of claim 1, e.g., an IFFT that itself is adapted to circularly shift input data by m samples, rather than relying on a circular shift performed prior to input to the IFFT, claim 1 as presently amended is believed allowable.

Claim 21 depends from claim 17. Claim 17 is believed allowable for the reasons set forth below, and claim 21 is believed allowable because it depends from an allowable base claim.

Claim 22 claims a method comprising, among other things, performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information without multiplying input samples by rotator coefficients. Mazzoni does not disclose the method claimed in claim 22 because Mazzoni performs a Fourier transform on a data samples that were previously rotated by multiplying the data samples with rotator coefficients. As set forth above with respect to the discussion of the rejections based on 35 U.S.C. §112, one aspect of the present invention involves modifying an IFFT pipeline so that the circular rotation is achieved within the IFFT pipeline,

and not prior to the transform circuitry. Claim 22 is therefore allowable over Mazzoni and the prior art disclosed in the application.

Claims 2, 18, and 23 were canceled by a previous amendment.

Claims 3, 10 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art and further in view of Walton et al., U.S. Pub. No. 2004/0081131. Applicants respectfully traverse the rejection.

Claim 3 depends from claim 1 and is believed allowable for the same reason as claim 1, that is, neither Mazzoni nor the prior art identified in the application teaches or discloses an Inverse Fast Fourier Transform circuit that is itself adapted to circularly shift the input data by m samples, rather than relying on a circular shift performed prior to input to the IFFT. Walton does not fill the gaps in Mazzoni. Accordingly, claim 3 is believed allowable.

Claim 10 is believed allowable because it depends from allowable based claims 1 and claim 3. Claim 10 further claims a particular example of the present invention, where the length of N samples of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples. Claim 11 depends from claim 10 and further claims a particular example of the present invention where the N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16. These specific examples are not obvious, and are examples which allow implementation of circular shifting by modifying the IFFT pipeline. These claims are believed allowable for these additional reasons.

Claims 4, 5, and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art, further in view of Walton, and further in view of Yeh, U.S. Pub. No. 2004/0059766. Applicants respectfully traverse the rejection.

Claims 4, 5 and 6 depend from claim 1, and therefore include all of the limitations of claim 1 and are believed allowable for the same reasons as independent claim 1. The remarks with respect to claim 1 are incorporated herein by reference.

Additionally, claim 4 recites that the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits with

memory and modifying the control for rotator circuits. Claim 5 recites the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory. As set forth above, neither Mazzoni, Walton, nor the prior art disclosed in the present application teach or suggest modifying an IFFT to circularly shift the data by m samples. Yeh also fails to fill the gaps in Mazzoni, Walton and the prior art disclosed in the present application. In particular, Yeh does not teach or disclose a transform circuit that is adapted to circularly shift input data by m samples by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory. Accordingly, neither Mazzoni, Walton, nor the prior art disclosed in the present application, nor Yeh teaches or suggests the specific ways that the IFFT is modified as recited in claims 4 and 5, i.e., by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits (claim 4) or by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory (claim 5). Accordingly, claims 4 and 5 are believed allowable for these additional reasons.

Claim 6 recites another configuration of the IFFT to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m samples. In particular, claim 6 recites a control circuit configured to modify the control to the rotator circuit and to selectively control the plurality of butterfly circuits whether the addition operation or the subtraction operation is output first in time. As set forth above, the cited passages of the cited references do not disclose such structure. In particular, with reference to the citation to Yeh, it is not relevant that Yeh discloses conventional butterfly circuits because Yeh does not disclose or suggest changing the order of the operation of conventional butterfly circuits to achieve a circular shift, as disclosed in the present application and claimed in claim 6. Claim 6 is allowable for this additional reason.

Claim 17 stands rejected as being unpatentable over Yeh in view of prior art disclosed in the present application. Applicants respectfully traverse the rejection.

Claim 17 recites a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by rotator coefficients. The discussion above relating to the rejections

based on 35 U.S.C. §112 is incorporated herein by reference. Yeh in view of disclosed prior art does not render claim 17 obvious because Yeh and the disclosed prior art, either alone or combined, do not teach or suggest a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information without multiplying input samples by rotator coefficients. Accordingly, claim17 is believed allowable.

Claims 19, 20, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art and further in view of Yeh. Applicants respectfully traverse the rejection.

Claims 19 and 20 depend from claim 17, and therefore include all of the limitations of claim 17 and are believed allowable for the same reasons as independent claim 17. The remarks with respect to claim 17 as set forth above are incorporated herein by reference.

Claims 24 and 25 depend from claim 22, and therefore include all of the limitations of claim 22 and are believed allowable for the same reasons as independent claim 22. The remarks with respect to claim 22 as set forth above are incorporated herein by reference.

Claim 19 recites that the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying a control for the first rotator circuit and memory contents of the first multiplier circuit with memory. As set forth above, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh teach or suggest a means for performing a circularly rotated Inverse Fast Fourier Transform that includes modifying an IFFT to circularly rotate the data. Accordingly, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh can teach or suggest the specific ways that the IFFT is modified as recited in claim 19, i.e., modifying a control for the first rotator circuit and memory contents of the first multiplier circuit with memory. Claim 24 is believed patentable for similar reasons.

Claim 20 recites that the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits. As set forth above, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh teach or suggest a means for performing a circularly rotated Inverse Fast Fourier Transform that includes modifying an IFFT to circularly rotate the data. Accordingly, neither Mazzoni, nor the prior art

disclosed in the present application, nor Yeh can teach or suggest the specific ways that the IFFT is modified as recited in claim 19, i.e., by modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits. Claim 25 is believed patentable for similar reasons.

Claims 26-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni. Applicants respectfully traverse the rejection.

Claim 26 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit. Claim 30 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to the butterfly circuit, modifying the control to the rotator circuit and re-ordering the memory contents of the multiplier circuit. As set forth above, Yeh and Mazzoni do not teach or suggest such structure. In particular, Mazzoni appears to rely on an external multiplier to multiply inputs to the IFFT by rotator coefficients before the data samples are entered into the transform circuit. Yeh, on the other hand, appears to re-order data using a "reordering circuit 1100," which is disclosed as a dual port RAM, to change the order of samples. Neither Mazzoni nor Yeh teach or disclose modifying a transform circuit to achieve a circular shift. Accordingly, claims 26 and 30, and the claims 27-29 and 31-33 that depend therefrom, are believed allowable over those published applications.

Claims 13-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni and further in view of the prior art disclosed in the present application. Applicants respectfully traverse the rejection.

Claim 13, as presently amended, recites that the Inverse Fast Fourier Transform circuit has a length of N samples, where N is a power of 2 and the N samples are not multiplied by rotator coefficients. Claim 13 also recited that the Inverse Fast Fourier Transform circuit has a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and is configured to circularly shift output information by m samples. The discussion above with respect to the rejections based on 35 U.S.C. §112 is incorporated by reference.

Claim 13 is patentable over Yeh and Mazzoni because neither Yeh, Mazzoni nor the prior art disclosed in the present application teach or suggest configuring an IFFT to circularly shift data by m

samples without multiplying the IFFT inputs by rotator coefficients. Furthermore, Yeh, Mazzoni nor the prior art disclosed in the present application teach or suggest configuring an IFFT having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and is configured to circularly shift output information by m samples. Accordingly, claim 13, and claims 14-16, which depend from claim 13, are believed allowable over the cited references.

Respectfully submitted,

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January 25, 2008

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